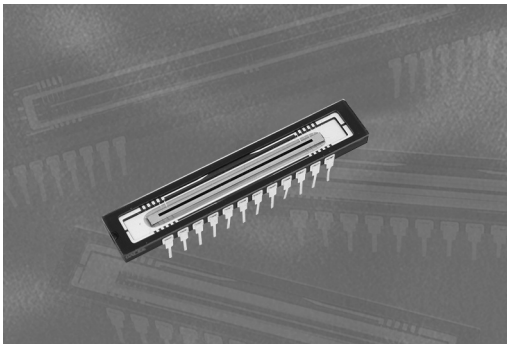
DALSA IL-C6 Image Sensor

Tall pixels (38:1 aspect ratio), tremendous dynamic range, great full-well capacity and a single output at up to 15MHz make the IL-C6 an outstanding performer in spectroscopic and specialized industrial applications.



Features

- Single output, up to 15MHz data rate
- 13µm (H) x 500µm (V) pixel size
- Photodiode photoelements
- 2048 elements
- Antiblooming and exposure control

Overview

DALSA's IL-C6 linear CCD image sensor uses TURBO-SENSOR™ technology to provide output at up to 15MHz. The sensor employs buried channel CCD shift registers to maximize output speed and reduce noise. The dynamic range of the IL-C6 is 6000:1 and provides output which has a linear dependence on light level up to saturation. Exposure control is incorporated to allow integration times shorter than the readout times if desired.

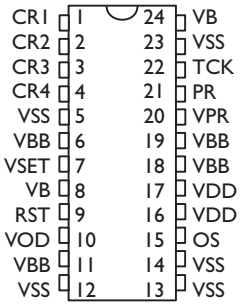
The IL-C6 sensor is ideally suited for high resolution spectroscopy applications requiring high sensitivity, providing nearly 2000 pixels per inch. Typical applications include:

- High resolution spectroscopy
- Inspection
- Bar code scanning
- Gauging and measurement

Physical Characteristics	IL-C6
Pixel dimensions	13µm x 500µm
Aperture	26.6mm x 0.5mm
Active pixels	2048
Isolation pixels per line	5
Light-shielded pixels per line	4

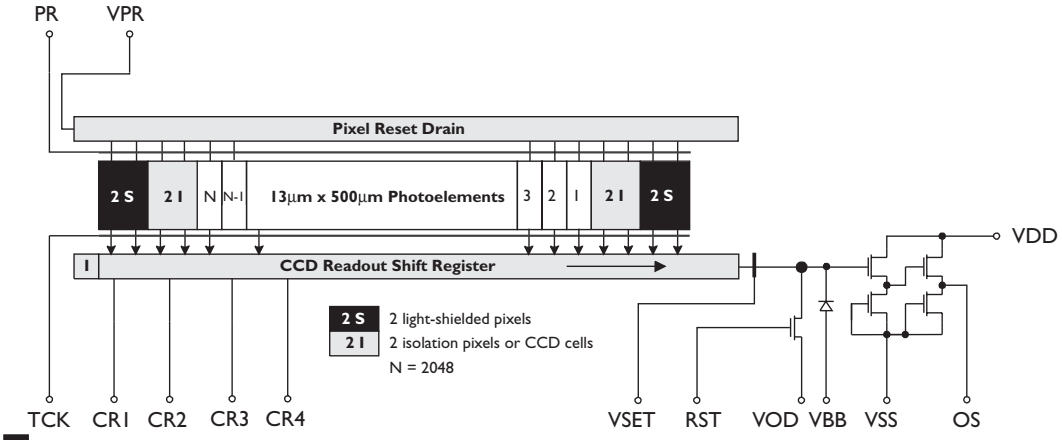
Table 1. IL-C6 Pin Functional Description

Pin	Symbol	Name
1	CR1	Readout Clock, Phase 1
2	CR2	Readout Clock, Phase 2
3	CR3	Readout Clock, Phase 3
4	CR4	Readout Clock, Phase 4
5,12-14,23	VSS	Ground Reference
6,11,18,19	VBB	Substrate Bias Voltage
7	VSET	Output Node Set Voltage
8,24	VB	Bias Voltage, Connect to VDD
9	RST	Output Reset Clock
10	VOD	Output Drain Bias Voltage
15	OS	Output Signal
16,17	VDD	Amplifier Supply Voltage
20	VPR	Pixel Reset Bias
21	PR	Pixel Reset Clock
22	TCK	Transfer Clock



CAUTION! These devices are sensitive to damage from electrostatic discharge (ESD). The leads should be shorted together during storage or handling to prevent damage to the device.

Figure 1. IL-C6 Image Sensor Block Diagram



1 Relative position of package Pin 1

Functional Description

The IL-C6 sensor is composed of three main functional groups: photodiodes in which the charge packets are generated; a single CCD readout shift register; and an output amplifier where the charge packets are converted to voltage pulses.

Detection

The IL-C6 sensor consists of a line of 2048 photodiodes which are 13µm by 500µm for a photosensitive area of 6,500 square micrometers. Light incident on these pixels is converted into charge packets whose size (i.e. the number of electrons) is linearly dependent upon the light intensity and integration time. When exposure control is enabled, the integration time is the time period between the falling edge of PR to the falling edge of the next TCK pulse. With exposure control disabled, the integration time is the time period between the falling edge of TCK to the falling edge of the next TCK pulse. Antiblooming is achieved by biasing the PR gate to a voltage between 0 and the TCK HIGH level so that only electrons beyond a certain packet size are drained away. There are two light-shielded and two isolation pixels at the beginning and end of the photoelement region.

Transfer

A four phase CCD buried channel shift register is employed to serially shift the charge packets to the output amplifier. The transfer clock (TCK) controls the transfer of signal from the photodiodes into phase CR1 of the CCD shift register. The HIGH voltage on this clock line should be equal to the HIGH voltage on the transport clocks. There is an isolation CCD pixel at the end of the readout shift register which must be considered when clocking the sensor.

Output

The signal charge packets from the readout shift register are transferred serially from the CR3 phase, over the SET gate (VSET bias), to the floating sense diffusion. As the signal charge is received, the corresponding potential on the diffusion is applied to the input of a two stage low noise amplifier, producing an output signal voltage on OS. The floating sense diffusion is cleared of signal charge by the reset gate (RST) to a voltage level equal to the potential on the output drain diffusion (VOD) in preparation for the subsequent signal charge packet. AC coupling to the output is recommended to eliminate the DC offset.

Table 2. IL-C6 Absolute Maximum Ratings

Specification	Unit	Min.	Max.
Voltage between VBB and any other pin	V	0	16
Storage Temperature	°C	-20	80
Operating Temperature	°C	-20	60

WARNING: Exceeding these values will void product warranty and may damage the device.

Table 3. IL-C6 AC Operating Conditions

Symbol	Name		Unit	Min.	Rec.	Max.
CR	Transport Clock, Readout Registers	offset*	V	0	0	0.5
		swing*	V	10	12	15
TCK	Transfer Clock	offset	V	VBB	0	0.5
		swing	V	10	12	15
RST	Reset Clock	offset	V	0	0	0.5
		swing	V	10	12	15
PR	Pixel Reset Clock	offset [1]	V	VBB	0	0.5
		swing [2]		10	12	15
f_{RST}	Reset Frequency		MHz		15	15
f_{DATA}	Data rate		MHz		15	15
f_{LINE}	Line rate		kHz			7.2

Notes: When the sensor is operated at the "Recommended" operating conditions, you may expect the "Typical" performance specifications listed in this data sheet

1. With antiblooming disabled. Increasing PR offset will increase the level of antiblooming (range 1-12V).
2. Recommended PR high level ≃ TCK high level.

Table 4. IL-C6 DC Operating Conditions

Symbol	Name	Unit	Min.	Typ.	Max.
VDD	Amplifier Supply Voltage	V	13	13.5	15
VBB	Substrate Voltage	V	-3	-1	0
VOD	Shift Register Drain Voltage	V	VSET + 7	13.5	VDD
VPR [1]	Pixel Reset Bias	V	13	VDD	15
VSET	SET Voltage	V	2	5	7
VB	Bias	V	13	13.5	15
VSS	Ground Reference	V		0	

Note: When the sensor is operated at the "Recommended" operating conditions, you may expect the "Typical" performance specifications listed in this data sheet.

1. With exposure control disabled. When EC is enabled, VPR must be adjusted for desired fat zero (range 7-15V).

Table 5. IL-C6 Input/Output Characteristics

Input Characteristics: Capacitance to VBB [1]	Unit	Typ.
From CRx	pF	240
From TCK	pF	75
From RST	pF	5
From PR	pF	75
Output Characteristics		
Output impedance (load-dependent)	Ω	300
DC output offset (V_{OFFSET})	V	8.5
Amplifier load current (I_{DD})	mA	20

Notes:

1. Using 1V pk-pk 1MHz signal with +10V DC offset.

Table 6. IL-C6 Performance Specifications

Specification	Unit	Min.	Typ.	Max.
VSAT	mV	1000	1500	
rms Noise	mV		0.25	0.30
Wavelength of peak responsivity	nm		750	
Peak responsivity	V/(μJ/cm²)	95	115	155
Dynamic range	ratio	3300:1	6000:1	
Noise Equiv. Exposure (NEE)	pJ/cm²		2.2	3.2
Saturation Equiv. Exposure (SEE)	nJ/cm²	8.7	13	
Charge Conversion Efficiency	μV/e^-	0.8	0.9	1.0
Full Well Capacity	ke^-	1100	1650	
Fixed Pattern Noise, exposure control disabled	mV		15	35
FPN, exposure control enabled	mV		15	35
Photoresponse Non-Uniformity, exposure control disabled	% OS		7.5	12
PRNU, exposure control enabled	% OS		10	17
Charge Transfer Efficiency (CTE)	%		0.99999	
Dark Signal @ 25°C ambient	mV			16

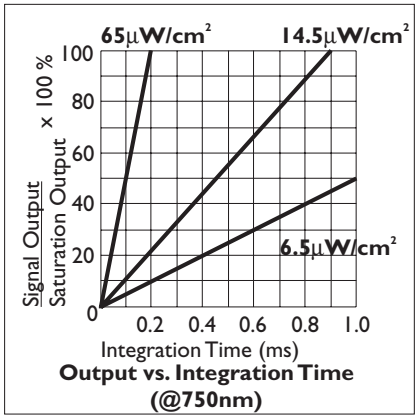
Notes:

- For explanations of specifications, refer to the Sensor Measurement Definitions document (doc# 03-36-00149).

Test Conditions:

- Tests conducted at f_{RST} = 7.5MHz, f_{DATA} = 7.5MHz, f_{TCK} =750Hz.
- Tungsten halogen light source, black body color temperature 3200K, filtered with 750nm IR cutoff filter.
- All measurements exclude the first and last pixel.
- Integration time (t_{int}) = 1.3ms.

Figure 2. IL-C6 Performance Measurements



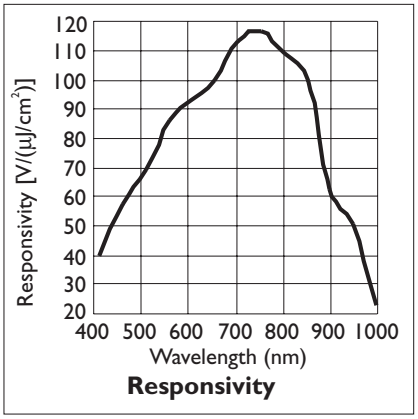
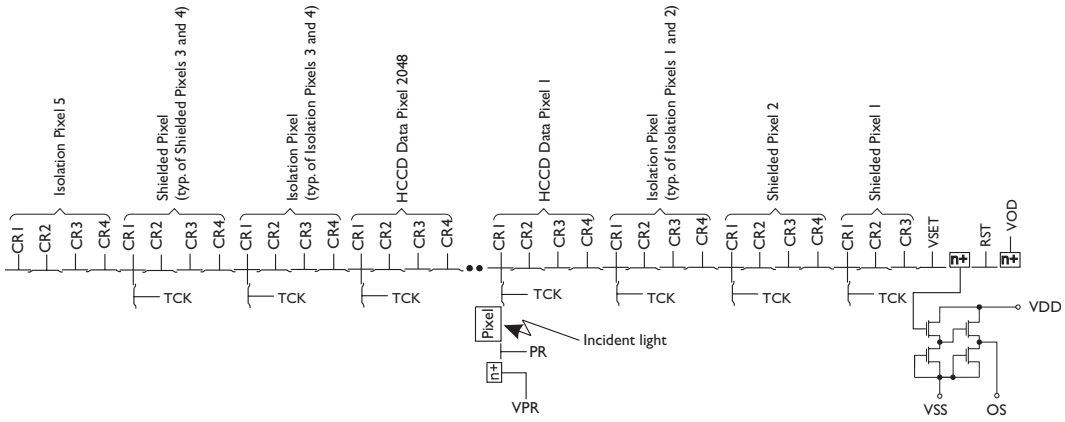


Table 7. IL-C6 Timing Parameters

Parameter	Description	Unit	Min.	Rec.	Max.
t_1	Integration time (exposure control disabled))				
t_2	Integration time (exposure control enabled)				
t_3	CR1 rising edge to TCK rising edge	ns	5		
t_4	TCK HIGH overlap with CR1 HIGH	ns	20		
t_5	TCK falling edge to CR1 falling edge	ns	2		
t_6	CR3 rising edge to RST rising edge	ns	0		
t_7	RST falling edge to CR3 falling edge	ns	0		
t_8	Adjacent CR clock HIGH overlap	ns	5		
t_9	RST HIGH duration	ns	15		

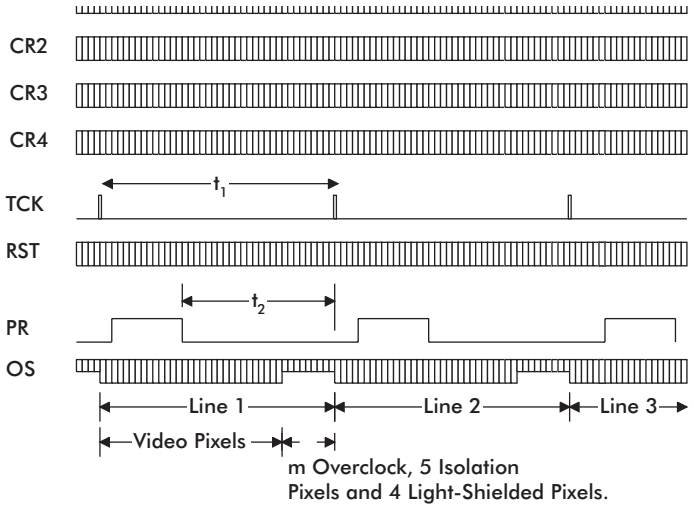
Figure 3. IL-C6 Gate Structure



ISO 9001 DALSA maintains a registered quality system meeting the ISO 9001 standard.

Life Support Applications
These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. DALSA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify DALSA for any damages resulting from such improper use or sale.

Figure 4. Overall Timing Diagram

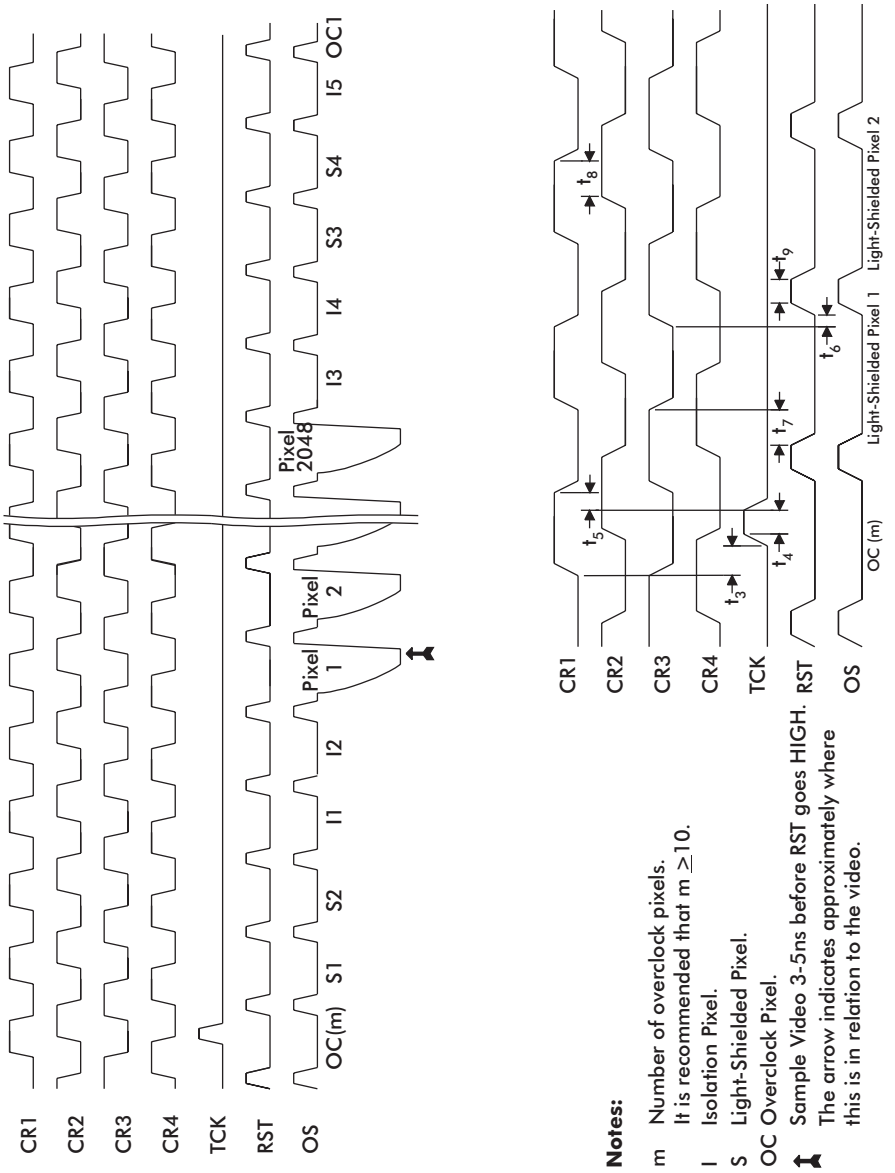


Notes:

m = Number of overclock pixels. It is recommended that m $\geq$10.

- PR must be synchronous with either CR1 or CR2.
- When exposure control is disabled, a short PR pulse (approx. 200ns) directly after the falling edge of TCK will reduce any image lag which may be present.

Figure 5. IL-C6 Detailed Timing



Notes:

m Number of overclock pixels.
It is recommended that m ≥10.

I Isolation Pixel.

S Light-Shielded Pixel.

OC Overclock Pixel.

Sample Video 3-5ns before RST goes HIGH.
The arrow indicates approximately where this is in relation to the video.

Figure 6. IL-C6 Sensor Operation Connections

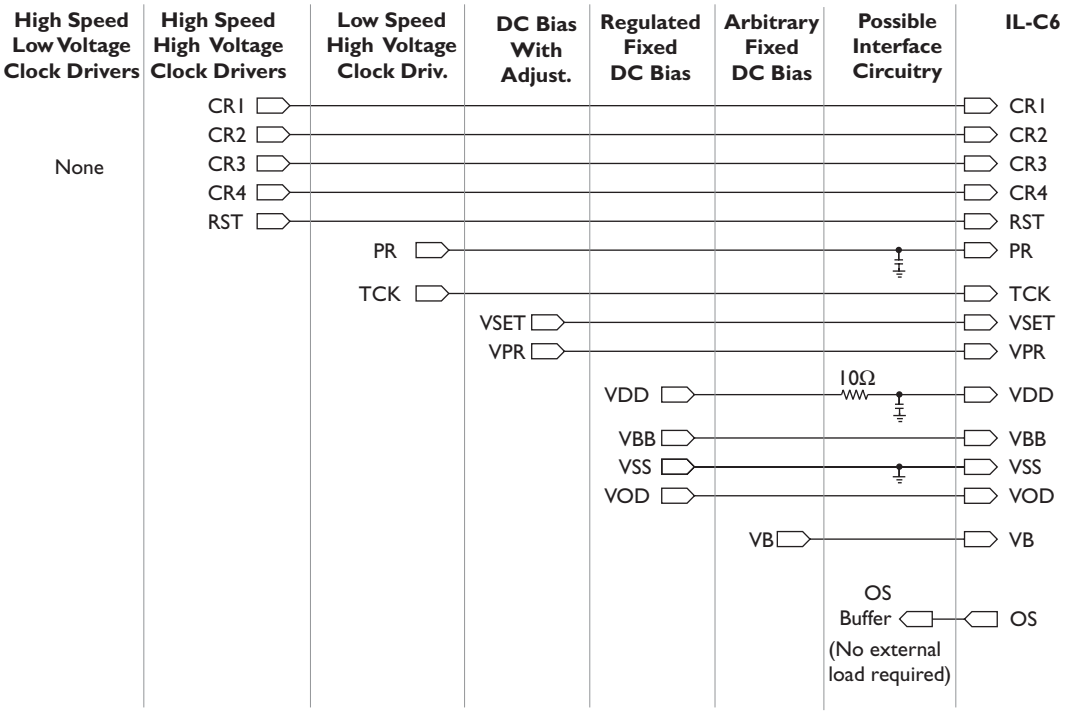


Figure 7. IL-C6 Package Dimensions