KAI - 1003M

1024 (H) x 1024 (V) Pixel

Megapixel Interline CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 3

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Eastman Kodak Company – Image Sensor Solutions - Rochester, NY 14650-2010
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1.1 Features

- **1 Megapixel Progressive Scan Interline CCD**
- **1024 (H) x 1024 (V) Imaging Pixels**
- **12.8 µm Square Pixels**
- **13.1 mm Square Imaging Area**
- **Microlenses for Increased Sensitivity**
- **Large capacity (170ke)**
- **Split Horizontal Register for 1 or 2 Outputs**
- **Binning to 1 x 2 or 2 x 2**

1.2 Description

The KAI-1003M is a high performance interline charge-coupled device (CCD) designed for a wide range of medical imaging and machine vision applications. The device is built using an advanced two-phase, double-polysilicon, NMOS CCD technology. The p+npn- photodiodes eliminate image lag while providing antiblooming protection and electronic shutter capability. The 12.8µm square pixels with microlenses provide high sensitivity and large dynamic range. The two output, split horizontal register and several binning modes enable a 15 to 60 frame per second (fps) video rate with this megapixel progressive scan imager.

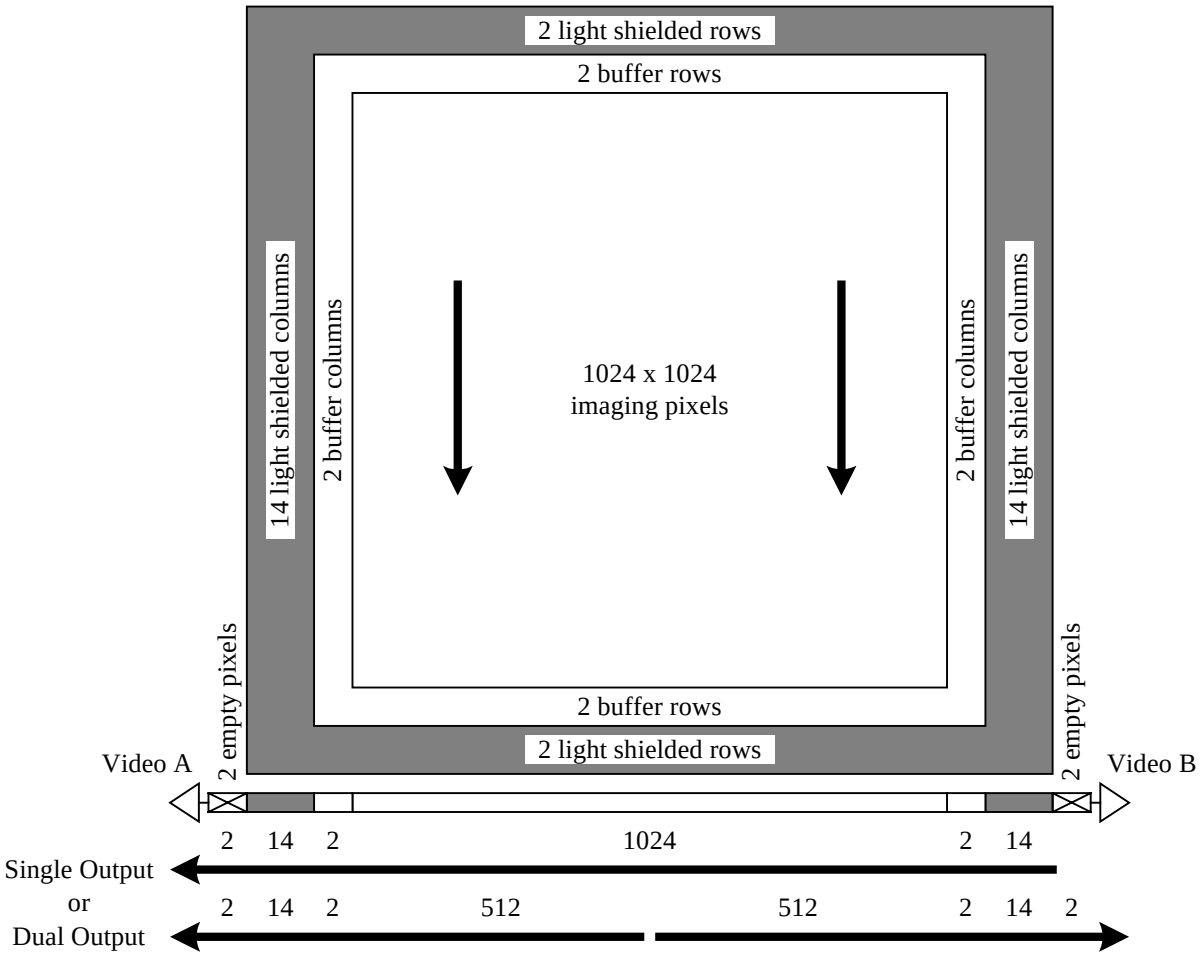

Figure 1 - KAI-1003M Pixel Architecture

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1.3 Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photodiode. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and integration time and nonlinearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming. The integration time can be decreased below the frame time by using an electronic shutter, which is a voltage pulse applied to the substrate to empty the photodiodes.

1.4 Charge Transport

The integrated charge from each photodiode is transported to the output by a three step process. The charge is first transferred from the photodiodes to the vertical shift registers by applying a large positive voltage to one of the vertical CCD phases. This transfer occurs simultaneously for all photodiodes. The charge is then transported from the vertical CCD registers to the horizontal CCD line by line in parallel. Finally, the horizontal CCD register transports each line of charge pixel by pixel serially to one or both of the output structures.

The single horizontal CCD register is split into two halves to allow a variety of line readout modes, as shown in Figsures 1 and 2. The A output half of the register is a true two-phase design, which results in unidirectional transport using phases H1A and H2A. The B output half of the register is a pseudo two-phase design, which allows bi-directional transport using phases H1B, H2B, H1C and H2C. Dual output is achieved with all of the first phases identical and all the second phases identical. If the clocks of H1A and H2A phases are shifted by one half cycle, the output remains dual with the outputs alternating, so that only one analog-to-digital converter is necessary. Finally, single output of the entire image from the A output is obtained by complementing the C phases, which reverses transport in the B half of the horizontal CCD.

Binning can be used in a 1x2 and a 2x2 mode. Two successive vertical transfers vertically bin the charge directly onto the horizontal CCD, as shown in Figures 11 and 12. Horizontal binning is accomplished by two successive horizontal transfers onto the H22 gate, which then transfers the charge to the output structure, as shown in Figure 13.

Combinations of output modes, binning and horizontal clock frequency allow the range of frame rates listed in Table 1.

1.5 Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and the FD is reset to the potential applied by the reset drain (RD). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the output pin of the device.

1.6 Non-Imaging Pixels

In addition to the 1024 (H) by 1024 (V) imaging pixels, there are active buffer, light shielded and empty pixels, as shown in Figure 1. A two pixel border of active buffer pixels surrounds the imaging area. These buffer pixels respond to illumination but are not tested for defects and non-uniformities. Two light shielded rows lead and follow each frame, and 14 light shielded columns lead and follow each line. The light shielded columns are tested for column defects and can be used for dark reference. Only the center 10 columns by 1028 rows of light shielded region on each side can be used for dark reference due to light leakage into the border of two pixels at the edges. Finally, two empty pixels occur at the beginning of each line, which are empty shift register cycles not associated with any vertical CCD columns. Empty pixels may also occur at the end of the line, depending on the timing.

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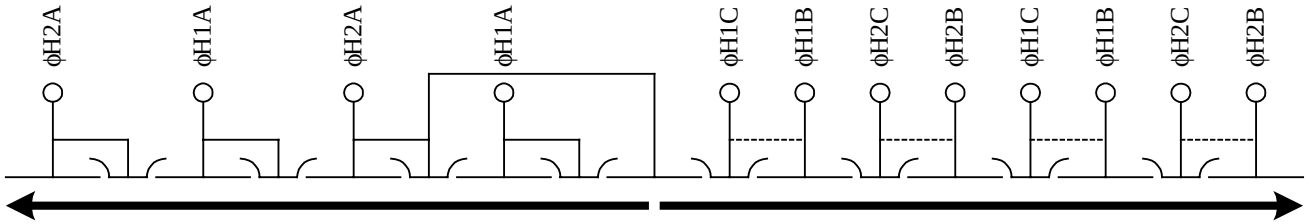
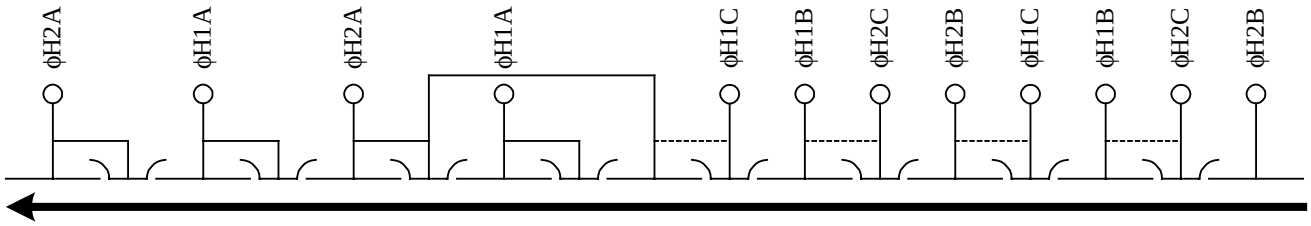


Dual Outputs

In phase	Out-of-phase
H1A = H1B = H1C	H1A - ½ = H1B = H1C
H2A = H2B = H2C	H2A - ½ = H2B = H2C



Single Output
H1A = H1B = H2C
H2A = H2B = H1C

Figure 2 - Horizontal CCD Registers

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Table 1 - KAI-1003M Calculated Clock Parameters

Binning (H x V)		1 x 1	1 x 2	2 x 2	2 x 2	1 x 1	Units
Output		Dual	Dual	Dual	Dual	Single	
HORIZONTAL CLOCK							
Frequency		20	20	20	40	20	MHz
Period	actual	50	50	50	25	50	ns
	effective	50	50	100	50	50	ns
Pixel counts	actual	532	532	532	532	1060	
	effective	532	532	266	266	1060	
VERTICAL TO HORIZONTAL TRANSFER (Horizontal Retrace Time)							
Equivalent H-clock counts (m)		80	80	80	160	80	
Duration		4.0	4.0	4.0	4.0	4.0	µs
HORIZONTAL LINE TIME							
Total H-clock counts		612	612	612	692	1140	
Line time		30.6	30.6	30.6	17.3	57.0	µs
VERTICAL CLOCK							
Line counts	actual	1032	1032	1032	1032	1032	
	effective	1032	516	516	516	1032	
PHOTODIODE READ (Vertical Retrace Time)							
Equivalent line counts (n)		4	4	4	7	2	
Duration		122.4	122.4	122.4	121.1	114.0	µs
FRAME RATE							
Total effective line counts		1036	520	520	523	1034	
Frame time		31.7	15.9	15.9	9.0	58.9	ms
Frame rate		31.5	62.8	62.8	110.5	17.0	frames/s

Notes:

- Time values have been rounded.
- The number of counts (n and m) shown here are nominal integers, but in general they do not need be integers. They can be adjusted for frame time, so long as the horizontal and vertical retrace times exceed the minimums specified in §3.6.
- Operation at 40MHz will have increased readout noise.

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2.1 Package Drawing

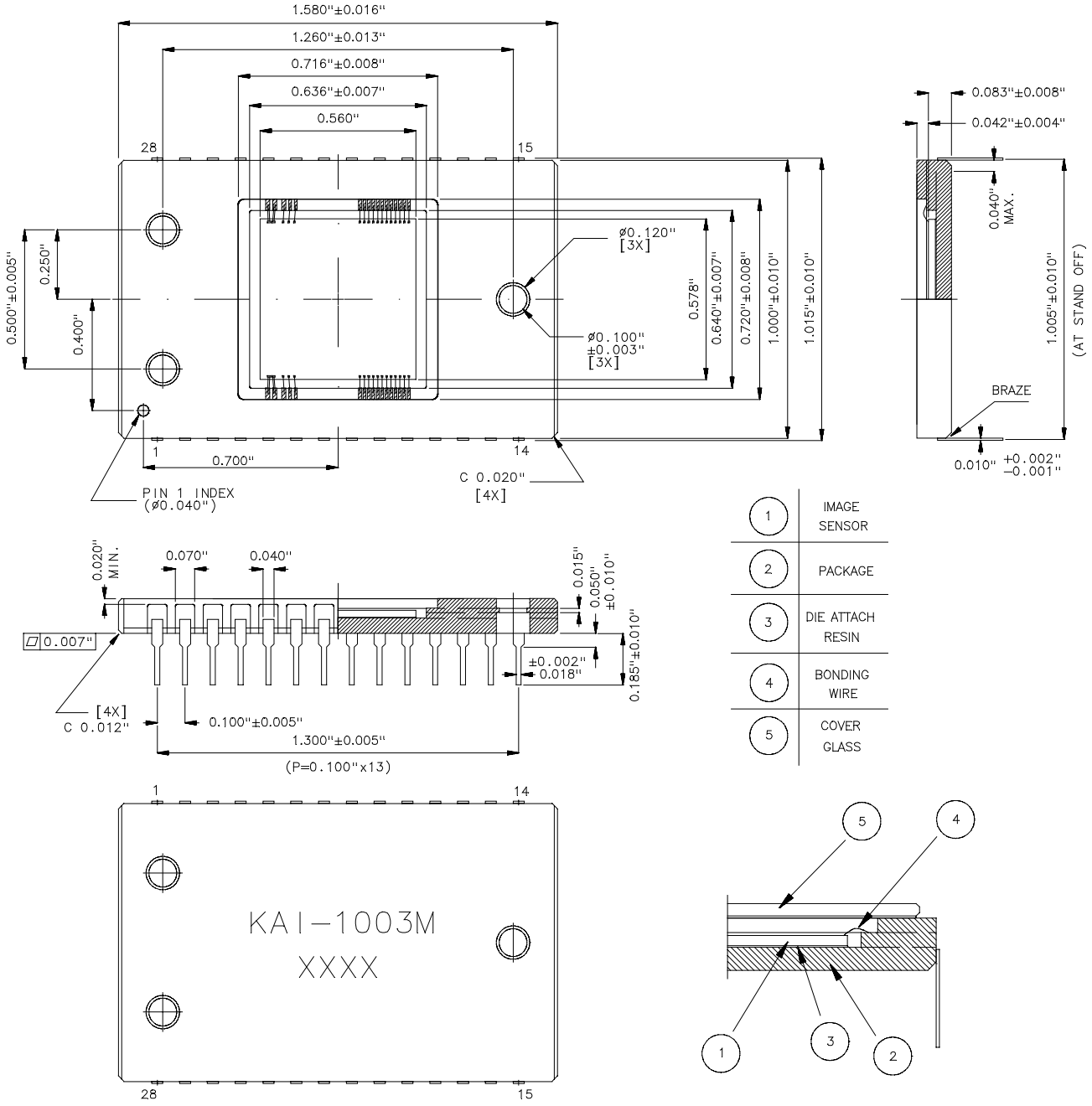

Figure 3 - Package Drawing

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2.2 Pin Description

Pin	Label
1	ϕV1
2	GND
3	SUB
4	VDD
5	VOUTA
6	VLG
7	RDA
8	ϕRA
9	OGA
10	SUB
11	ϕH1A
12	ϕH2A
13	ϕH22A
14	GND

Pin	Label
15	ϕH22B
16	ϕH2B
17	ϕH2C
18	ϕH1C
19	ϕH1B
20	OGB
21	ϕRB
22	RDB
23	VSS
24	VOUTB
25	VMIN
26	SUB
27	GND
28	ϕV2

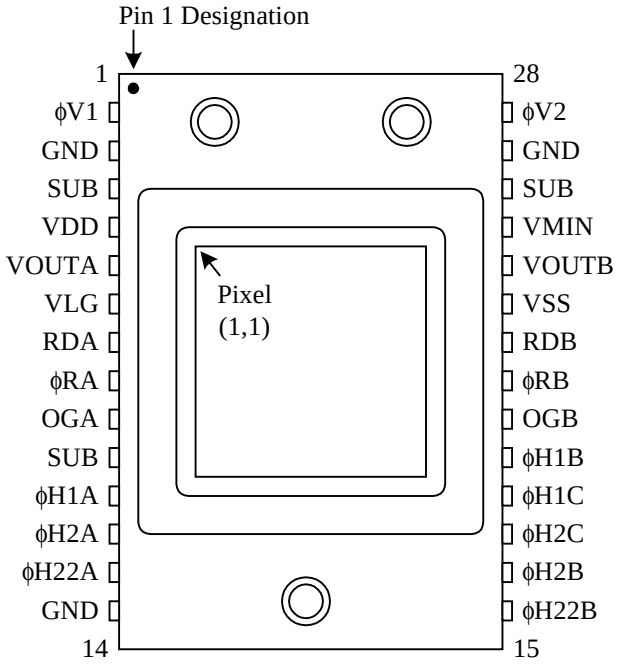

Figure 4 - Package Pin Designations - Top View

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2.3 Cover Glass Specification

Item	Specification
Substrate	Corning 7059 or equivalent
Thickness	0.030″ ± 0.002″
Coating	Double-sided anti-reflecting coating on a 0.660” x 0.660” square for a transmission minimum of 98% in the 400 to 700nm wavelength.
Scratch	No scratch greater than 10 microns

3.1 Absolute Maximum Ratings

Item	Description	Min.	Max.	Units	Notes
Temperature	Operation to Specification	0	40	°C	
	Operation Without Damage	-10	70	°C	
	Storage	-55	80	°C	
Relative Humidity	Operation Without Damage	0	95	%	1
Voltage (Between Pins)	SUB - GND	-0.6	50	V	2
	VRD, VSS, VDD - GND	-0.6	25	V	
	VMIN - GND	-15	0.6	V	
	All Clocks - GND		17	V	
	ϕV1 - ϕV2		17	V	3
	ϕH1 - ϕH2		17	V	
	ϕH1, ϕH2 - ϕV2		17	V	
	ϕH2 - OG		17	V	
	VLG, OG - GND		17	V	
Current	Output Bias Current (IDD)	----------	10	mA	4
Capacitance	Output Load Capacitance (CLOAD)	----------	10	pF	4

Notes:
1. Without condensation.
2. Under normal operating conditions, the substrate voltage should be maintained above 8.0 V. The substrate voltage should not remain above 25 V for longer than 100 µs.
3. Maximum of 20 V for ϕV1H - ϕV2L, with 20 µs maximum duration.
4. Each output.

Caution:	**This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance to strict ESD procedures for Class 1 devices.**

Caution:	**Improper cleaning of the cover glass may damage these devices. Refer to Application Note DS 00-009 "Cover Glass Cleaning Procedure for Image Sensors"**

3.2 DC Operating Conditions

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Output Gate	OG	1.8	2.0	2.2	V	
Reset Drain	VRD	10.0	10.5	11.0	V	
Output Amplifier Return	VSS		0.0		V	1
Output Amplifier Load Gate	VLG	1.4	1.5	1.6	V	
Output Amplifier Supply	VDD	14.5	15.0	15.5	V	
Disable ESD Protection	VMIN		-8.5		V	2
Substrate	VSUB	8.0	TBS	18.0	V	3,4
Ground, P-well	GND		0.0		V	4

Notes:
1. Current sink.
2. Connect a 0.001 µf capacitor between VMIN and GND. VMIN must be more negative than the low voltage of any of the ϕH clocks and should be established before the ϕH voltage is applied.
3. DC value when electronic shutter is not in use. See §3.2 for electronic shutter pulse voltage. The operating value of the substrate voltage, VSUB, will be supplied with each shipment.
4. Ground and substrate biases should be established before other gate and diode potentials are applied.

3.3 AC Clock Level Conditions

Description	Level	Symbol	Min.	Nom.	Max.	Units	Notes
Vertical CCD Clocks	High	ϕV2H	9.5	10.5	11.5	V	1
	Mid	ϕV1M, ϕV2M	-0.8	-0.5	0.0	V	1
	Low	ϕV1L, ϕV2L	-9.0	-8.5	-8.0	V	1
Horizontal CCD Clocks	High	ϕH1H, ϕH2H	4.5	5.0	5.5	V	1
	Low	ϕH1L, ϕH2L	-6.5	-6.0	-5.5	V	1
Reset clock	Amplitude	ϕRswing		5.0		V	
	Low	VϕRlow	0	TBS	5.0	V	2
Electronic Shutter Pulse	Shutter	VShutter	37	40	45	V	3

Notes:
1. For best results, the CCD clock swings must be greater than or equal to the nominal values.
2. Reset clock low level voltage will be supplied with each shipment.
3. Electronic shutter pulse voltage referenced to GND. See §3.2 for DC level when electronic shutter is not in use.

3.4 Electronic Shutter Operation

Electronic shuttering is accomplished by pulsing the substrate voltage to empty the photodiodes. See Figure 14 for timing. The pulse must not occur while useful information is being read from a line.

3.5 Calculated Clock Capacitance

Description	Phase	Symbol	Typical	Units	Notes
Vertical CCD Clocks	1 to GND	C ϕV1	55/37	nF	1
	2 to GND	C ϕV2	50/32	nF	1
	1 to 2	C ϕV1 - ϕV2	4	nF	
Horizontal CCD Clocks	1A	C ϕH1A	58/21	pF	1,2
	1B	C ϕH1B	41/13	pF	1,2
	1C	C ϕH1C	15/10	pF	1,2
	2A	C ϕH2A	48/22	pF	1,2
	2B	C ϕH2B	30/11	pF	1,2
	2C	C ϕH2C	18/13	pF	1,2
HCCD Summing Clock		C ϕH22A/B	3	pF	
Reset clock - GND		C ϕRA/B	5	pF	

Notes:
1. Accumulation/depletion capacitances.
2. Capacitance of this gate to GND and all other gates.

3.6 AC Timing Requirements

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Vertical High Level Duration	T_{V2H}	15		20	µs	
Vertical Transfer Time	T_V	1.0	2.0/1.0		µs	1
Vertical Pedestal Delay 1 & 3	T_{VPD1}, T_{VPD3}	40			µs	
Vertical Pedestal Delay 2	T_{VPD2}	15			µs	
Horizontal Delay	T_{HD}	1.5/0.5			µs	1
Reset Duration	T_R		10		ns	2
Horizontal CCD Clock Frequency	f_H		20		MHz	3
Pixel Time	T_H		50		ns	
Line Time	T_L					4
Frame Time	T_F					4
Clamp Delay	T_{CD}				ns	5
Sample Delay	T_{SD}				ns	5
Electronic Shutter Pulse Duration	T_{ES}	5	7.5	10	µs	
Electronic Shutter Horizontal Delay	T_{ESHD}	1.0			µs	

Notes:
1. Non-binning/binning times.
2. The rising edge of ϕR should be coincident with the rising edge of ϕH22, within ±5 ns.
3. Horizontal CCD clock frequency can be increased to 40MHz, with increased readout noise.
4. See Table 1 for nominal line and frame time in each mode.
5. The clamp delay and sample delay should be adjusted for optimum results.

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3.7 CCD Clock Waveform Conditions

Non-binning

Description	Phase	Symbol	twh	twl	tr	tf	Units	Notes
Vertical CCD Clocks	1	ϕV1M/L	-------	1.5	0.5	0.5	µs	
	2	ϕV2M/L	1.5	-------	0.5	0.5	µs	
	2, High	ϕV2H	15	-------	1.0	1.0	µs	
Horizontal CCD Clocks	1	ϕH1	20.5	21.5	4.0	4.0	ns	
	2	ϕH2	20.5	21.5	4.0	4.0	ns	
	2, Binning	ϕH22	20.5	21.5	4.0	4.0	ns	1
Reset clock		ϕR	5	39	3	3	ns	

2 x 2 Binning

Description	Phase	Symbol	twh	twl	tr	tf	Units	Notes
Vertical CCD Clocks	1	ϕV1M/L	0.5	0.5	0.5	0.5	µs	2
	2	ϕV2M/L	0.5	0.5	0.5	0.5	µs	2
	2, High	ϕV2H	15	-------	1.0	1.0	µs	
Horizontal CCD Clocks	1	ϕH1	20.5	21.5	4.0	4.0	ns	
	2	ϕH2	20.5	21.5	4.0	4.0	ns	
	2, Binning	ϕH22	46.0	46.0	4.0	4.0	ns	
Reset clock		ϕR	5	89	3	3	ns	

Notes:

- Typical values measured with clocks connected to image sensor device. The actual values should be optimized for particular board layout.

1. ϕH22 may be connected to ϕH2 in 1x1 mode.
2. twh and twl for ϕV1M/L and ϕV2M/L are the time periods during the double pulses.

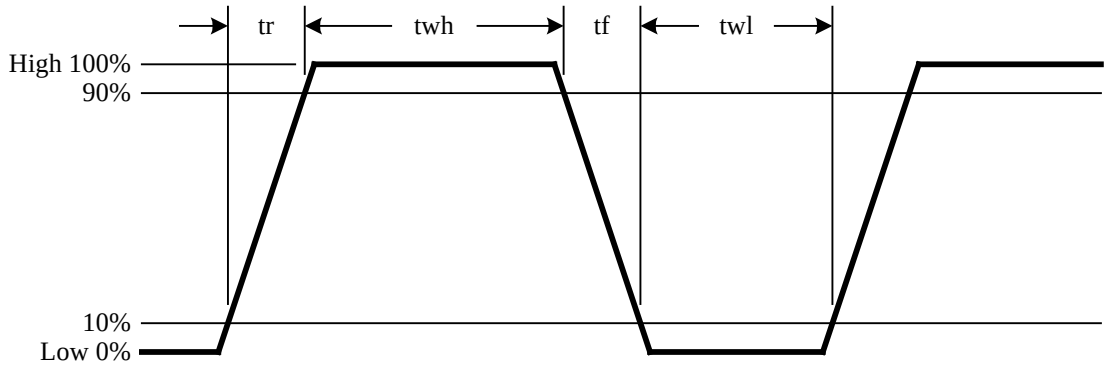

Figure 5 - CCD Clock Waveform

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Frame Timing - 1 x 1

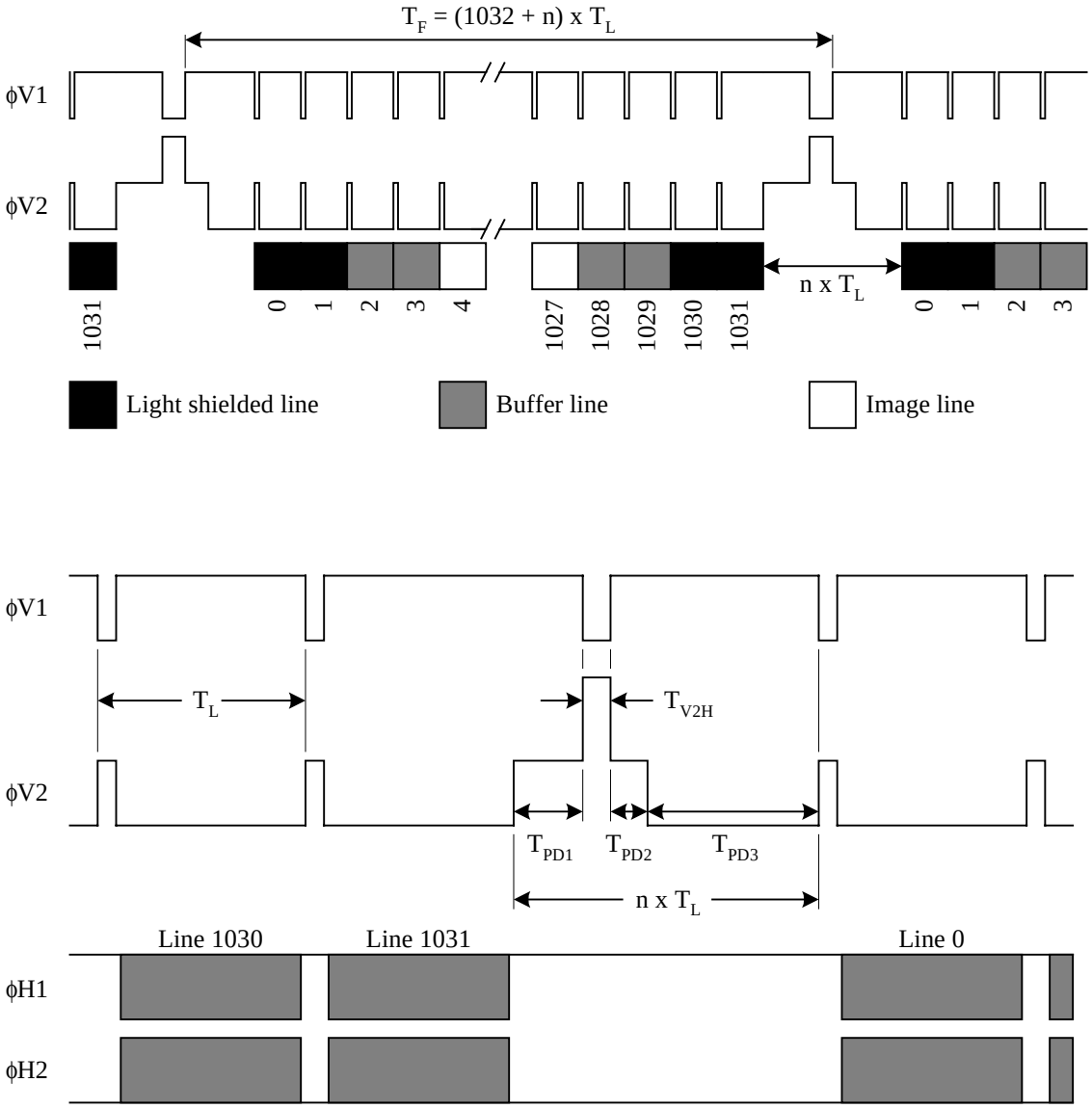

Figure 6 - Frame Timing - 1 x 1

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Line Timing - 1 x 1 - Dual Output, In-phase

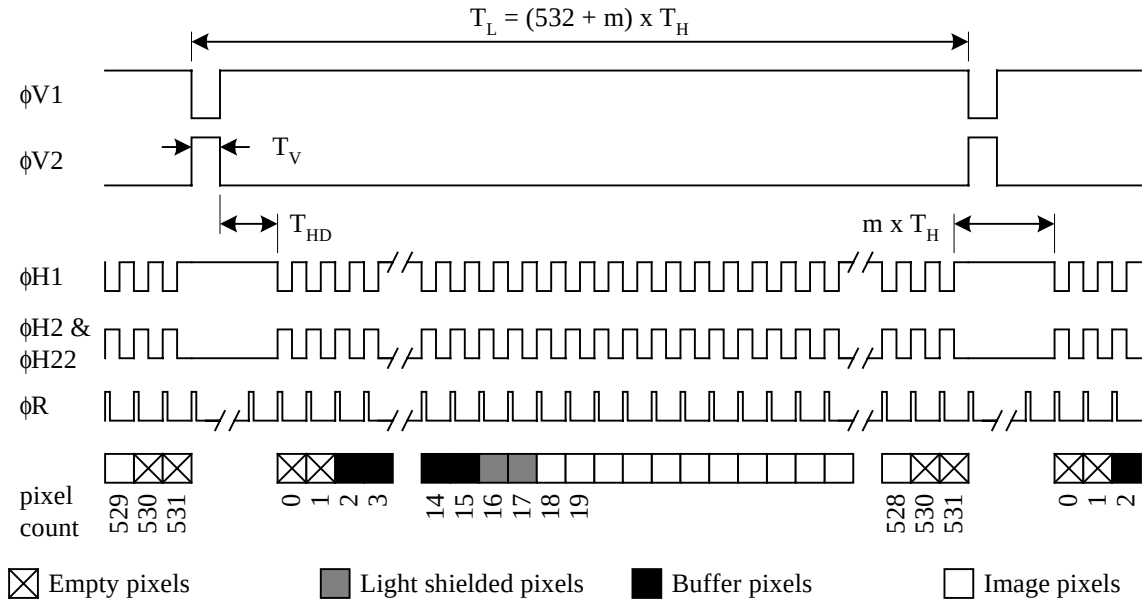

Figure 7 - Line Timing - 1 x 1 - Dual Outputs, In-phase

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Line Timing - 1 x 1 - Dual Output, Out-of-phase

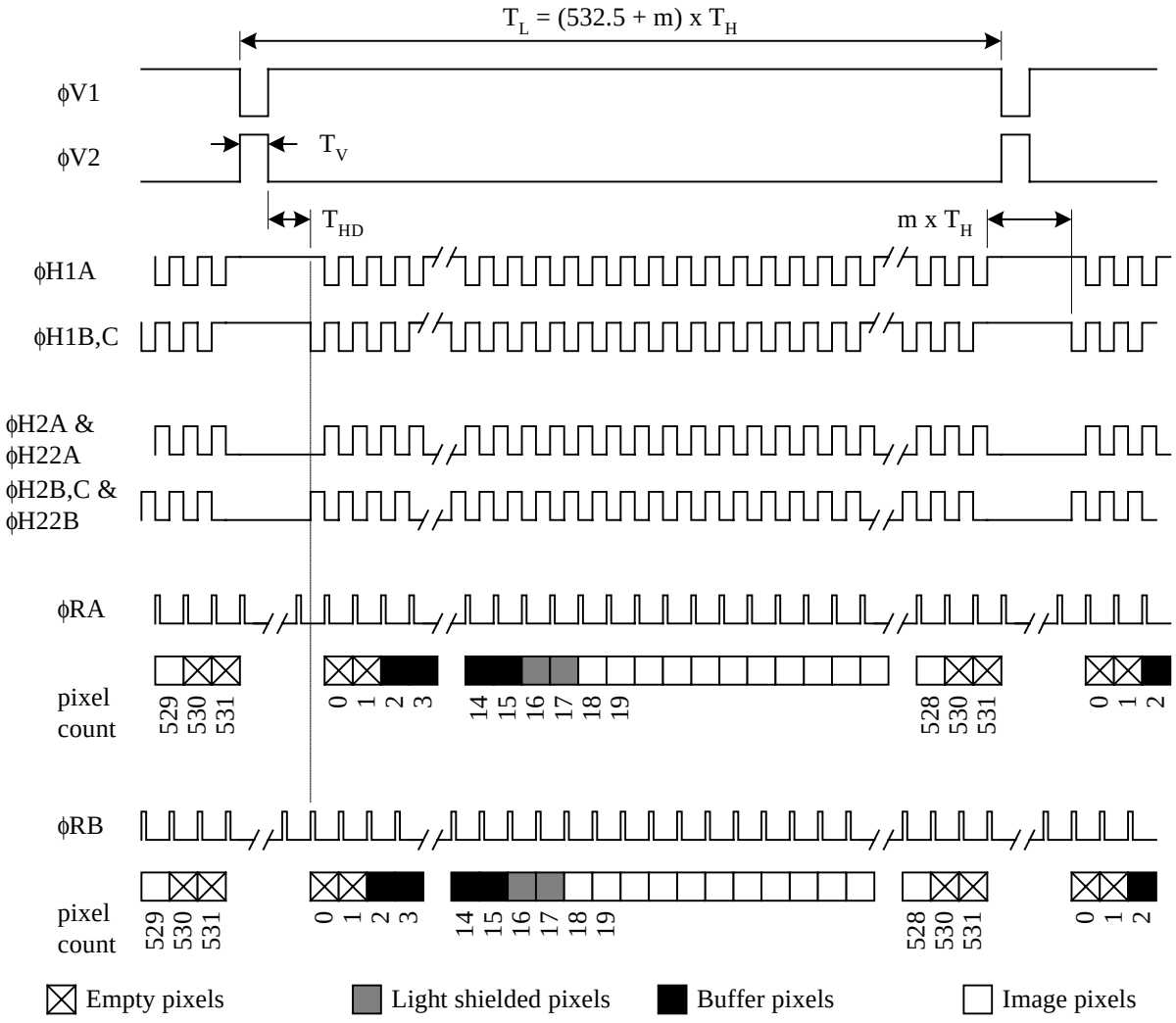

Figure 8 - Line Timing - 1 x 1 - Dual Outputs, Out-of-phase

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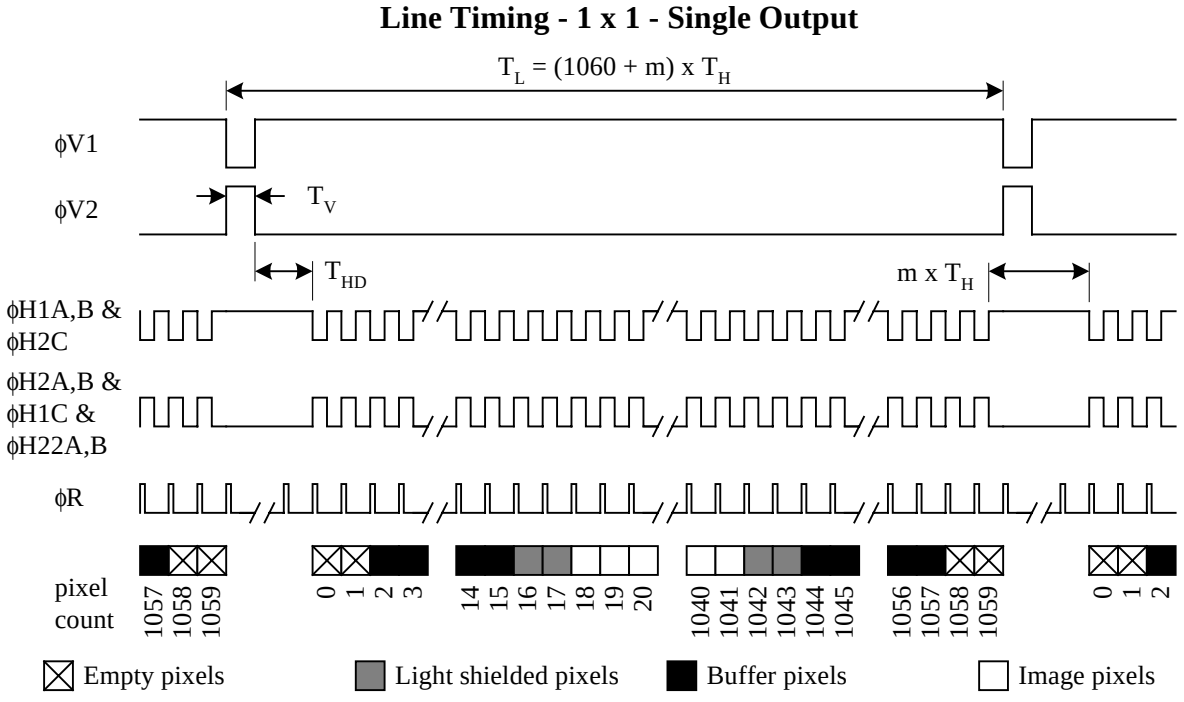

Figure 9 - Line Timing - 1 x 1 - Single Output

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Pixel Timing - 1 x 1

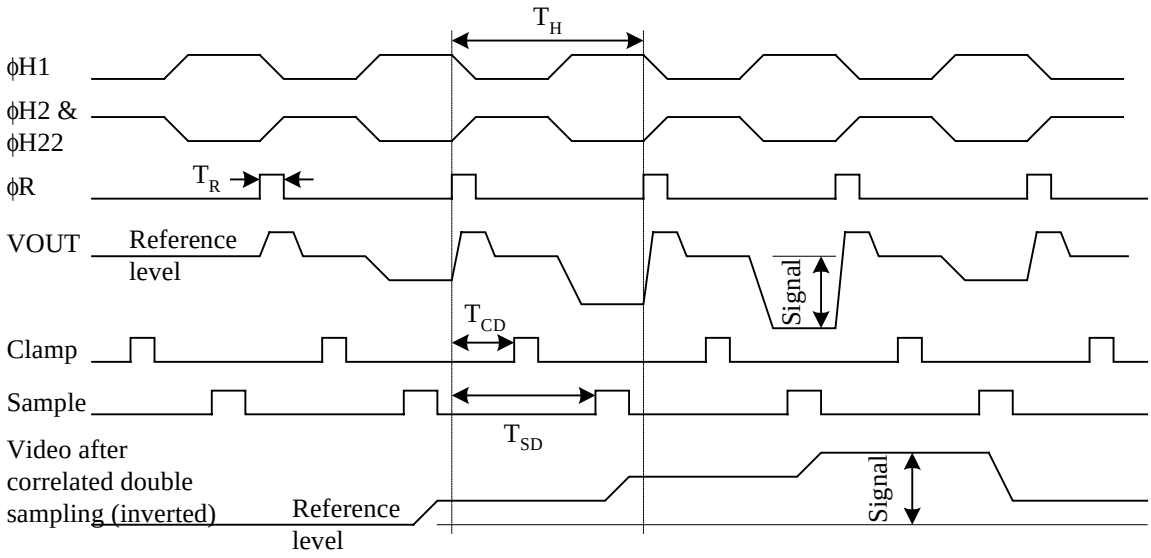

Figure 10 - Pixel Timing - 1 x 1

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Frame Timing - 2 x 2

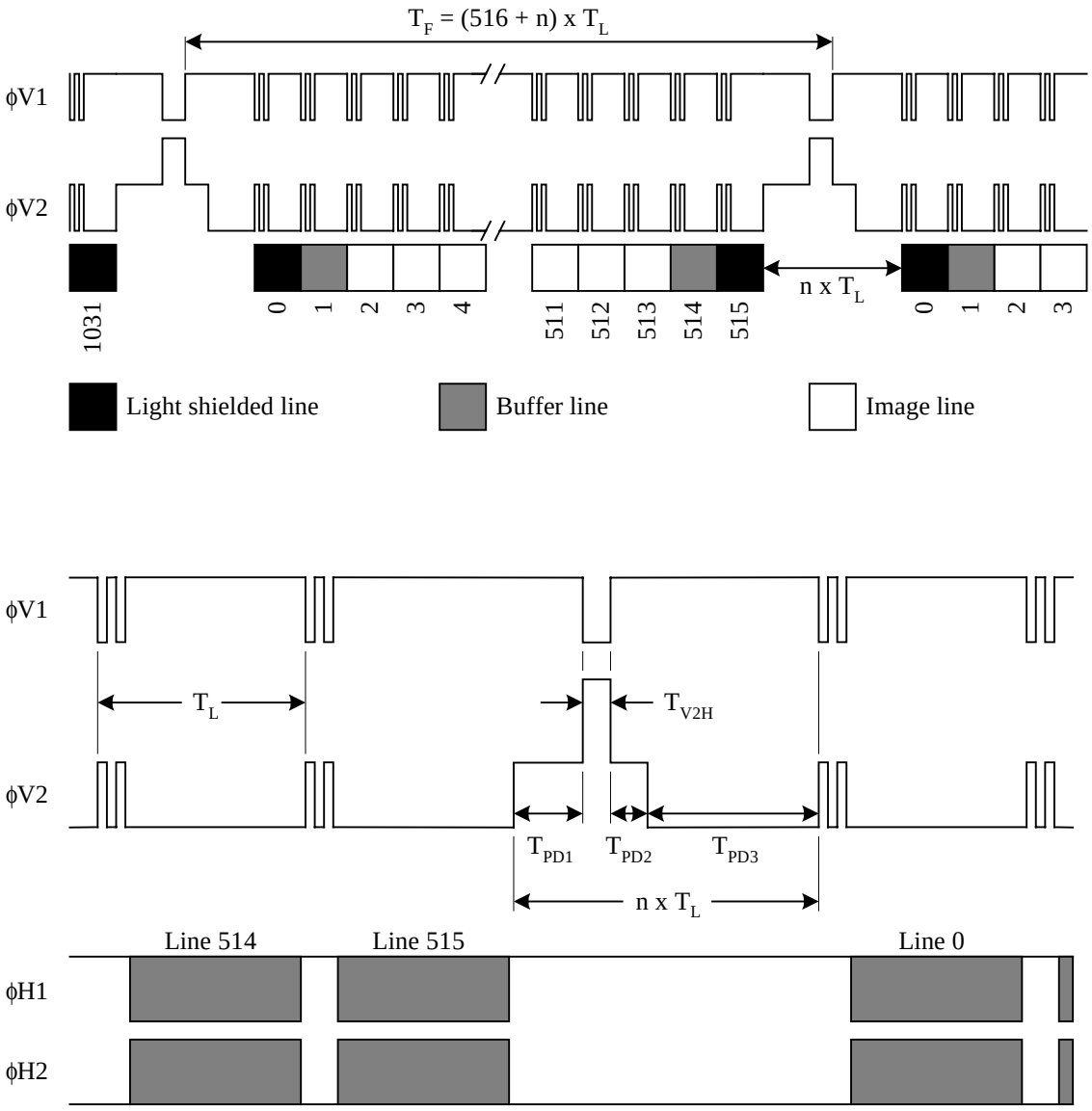

Figure 11 - Frame Timing - 2 x 2

Line Timing - 2 x 2

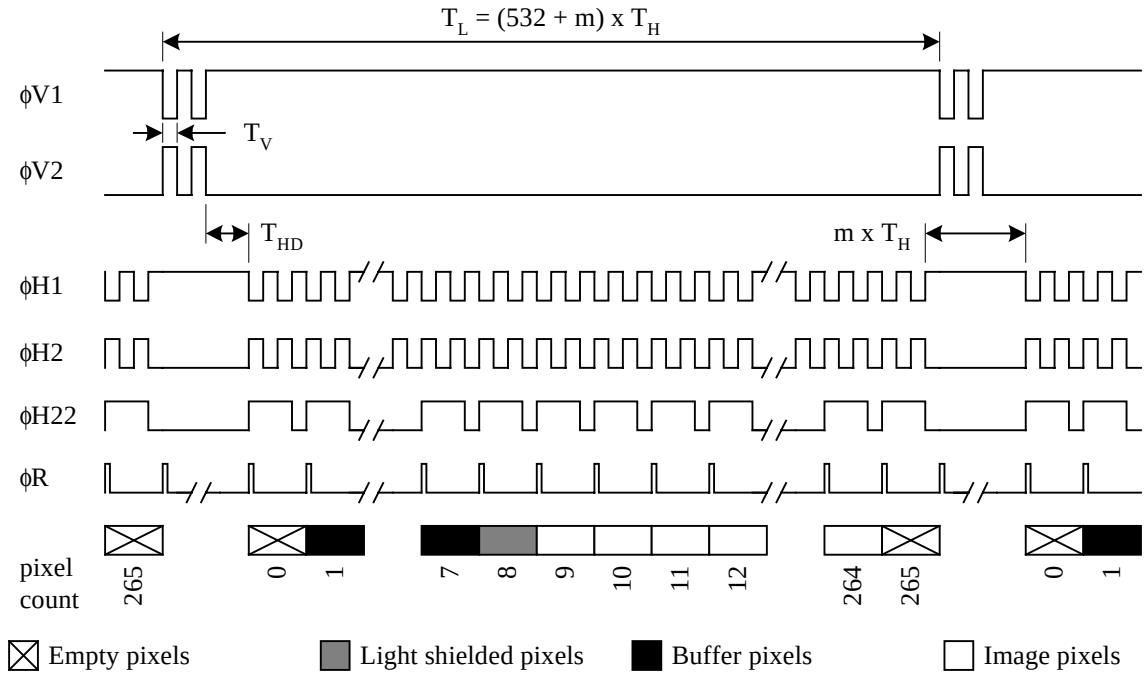

Figure 12 - Line Timing - 2 x 2

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Pixel Timing - 2 x 2

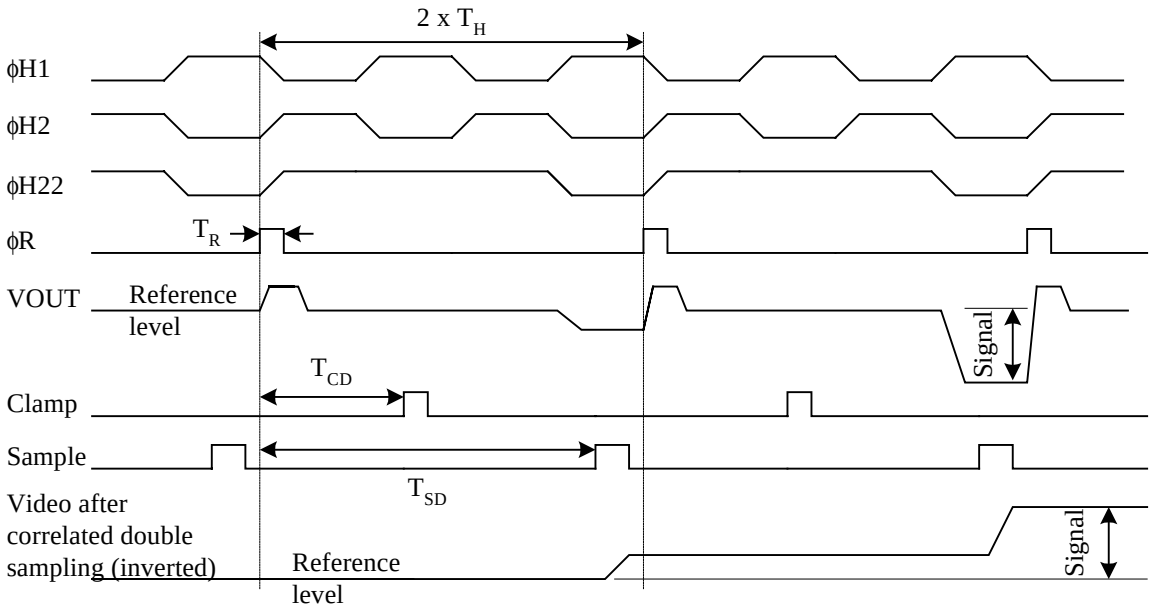
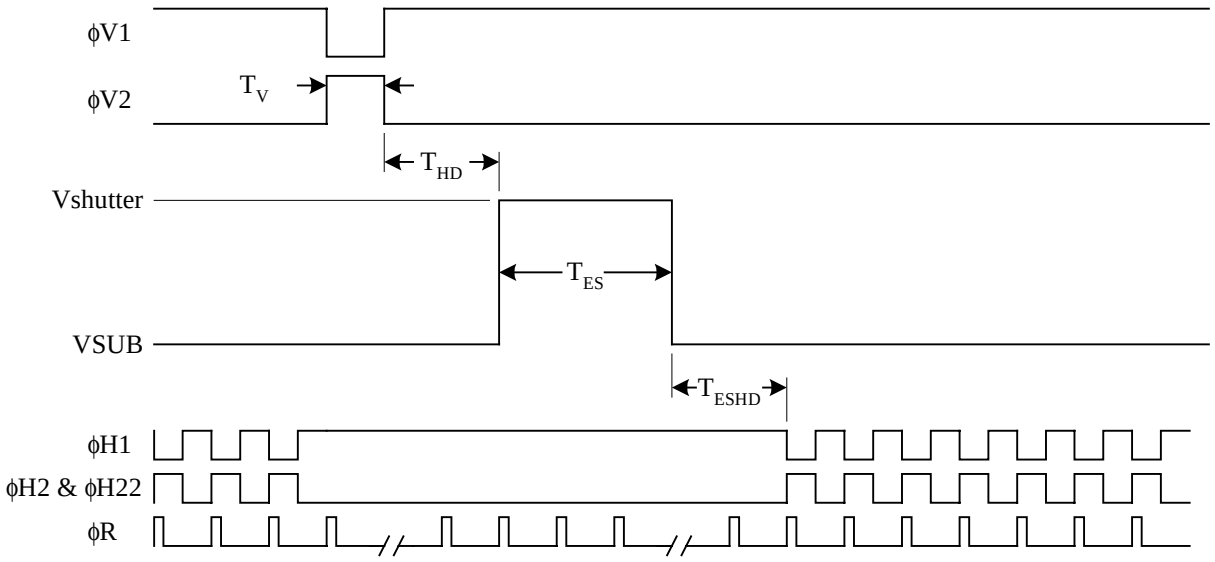


Figure 13 - Pixel Timing - 2 x 2

Electronic Shutter Line Timing



Integration Time Definition

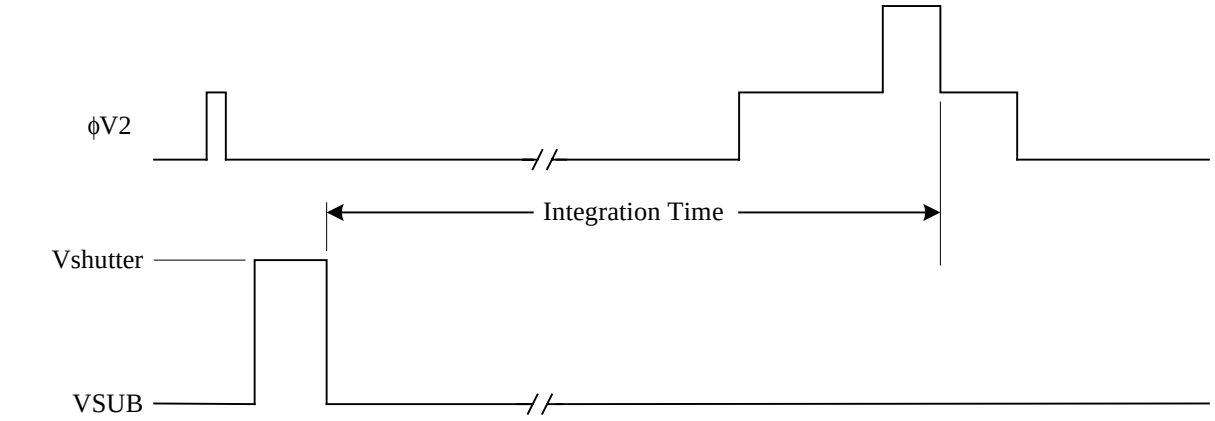


Figure 14 - Electronic Shutter Timing

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4.1 Performance Specifications

All values measured at 40°C and 30 frames/s (integration time = 33 ms) for nominal operating parameters unless otherwise noted. These parameters exclude defective pixels.

Description	Symbol	Min.	Nom.	Max.	Units	Notes
Saturation charge capacity with blooming control	Q_{sat}	170			ke	
Output gain		6.5	7.5	8.5	μV/e	
Output voltage at the saturation level	V_{sat}		1.3		V	
Quantum efficiency at 500 nm			32		%	
Quantum efficiency at 540 nm			30		%	
Quantum efficiency at 600 nm			24		%	
CCD readout noise with CDS			40	50	e rms	
Dark current	I_{dark}		0.25	0.45	nA/cm^2	
Antiblooming factor	X_{ab}	100				1, 2
Vertical smear			0.005	0.01	%	2, 6
Nonuniformity of sensitivity			0.3	0.5	% rms	3, 4
Nonuniformity of dark current			14		e rms	4
Output signal nonlinearity			1	2	%	5
Gain difference between the two video outputs				10	%	5
Nonuniformity of gain between the two outputs			0.5	1.5	%	5

Notes:
1. The illumination required to bloom the image sensor reported as a multiple of the saturation intensity. Blooming is defined as doubling the vertical height of a spot that is 10% of the vertical CCD height at the saturation intensity.
2. Measured with continuous green light centered at 550 nm, F/4 optics and a spot size that is 10% of the vertical CCD height.
3. Measured at 90% of 150 ke output.
4. Measured in the center 50 x 50 pixels.
5. Between 10% and 90% of 150 ke output.
6. Measured without electronic shutter operation.

4.2 Typical Quantum Efficiency

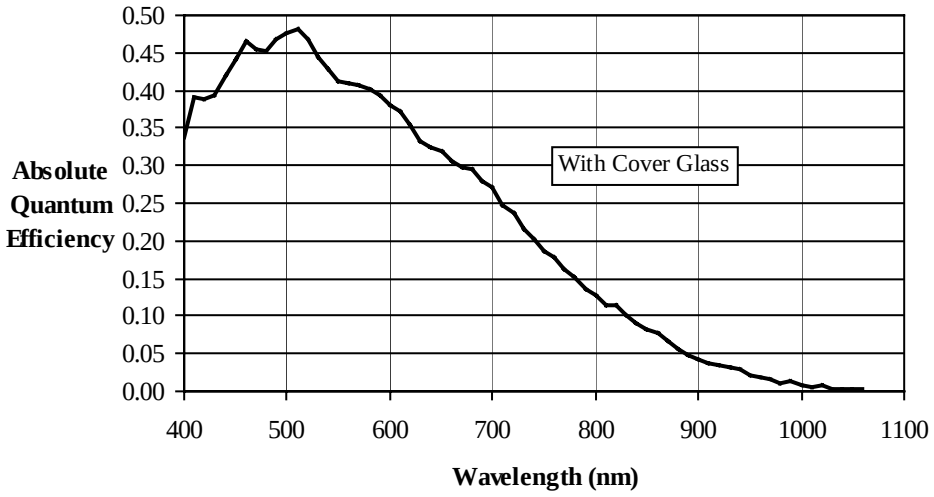

Figure 15 - Quantum Efficiency Spectrum

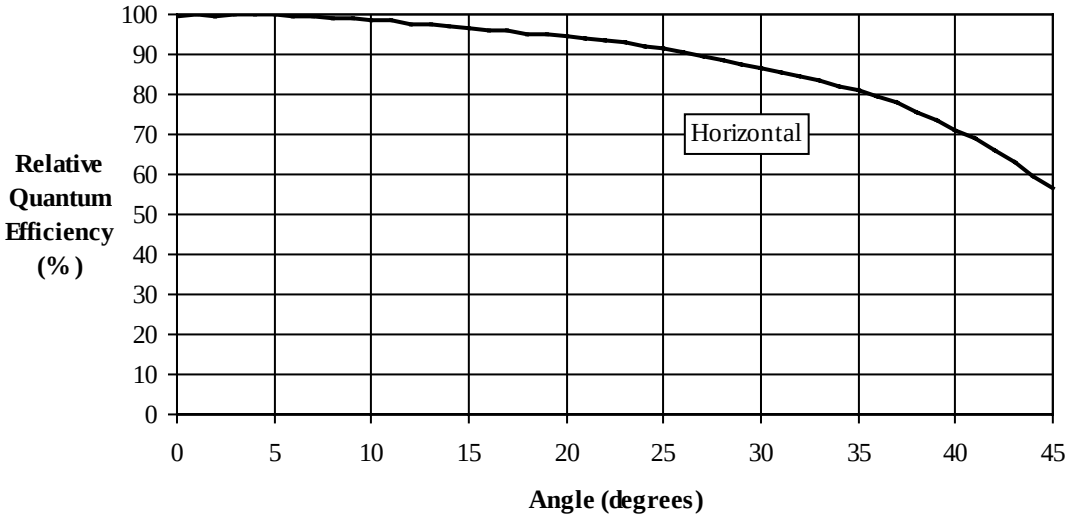

Figure 16 - Angular Dependence of Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

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4.3 Defect Specifications

Defect Test Conditions

Temperature	40°C
Integration time	33 ms (20 MHz HCCD frequency, no binning, 30 fps frame rate)
Light source	Continuous green light centered at 550 nm
Operation	Nominal voltages and timing

Defect Definitions

Name	Maximum Number	Definition
Major Defective Pixel	20	A pixel whose signal deviates by more than 25mV from the mean value of all active pixels under dark field condition or by more than 15% from the mean value of all active pixels under uniform illumination at 105ke$^-$ output signal.
Minor Defective Pixel	100	A pixel whose signal deviates by more than 8mV from the mean value of all active pixels under dark field condition.
Cluster Defect	4	A group of 2 to 6 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.
Column Defect	0	A group of more than 6 contiguous major defective pixels along a single column.

Defect Proximity

Minimum distance between defective clusters	2 pixels in all directions without major pixel defects
Minimum distance between defective columns	3 columns without column defects or cluster defects

5.1 Quality Assurance and Reliability

5.1.1 Quality Strategy: All devices will conform to the specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process.

5.1.2 Replacement: All devices are warranted against failures in accordance with the Terms of Sale.

5.1.3 Cleanliness: Devices are shipped free of contamination, scratches, etc. that would cause a visible defect.

5.1.4 ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe work stations.

5.1.5 Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions, and can be supplied upon request.

5.1.6 Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

5.2 Ordering Information

See Appendix 1 for available part numbers.

Address all inquiries and purchase orders to:

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Eastman Kodak Company
Rochester, New York 14650-2010
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Kodak reserves the right to change any information contained herein without notice. All information furnished by Kodak is believed to be accurate.

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

Appendix 1 Part Number Availability

Note:

This appendix may be updated independently of the performance specification. Contact Eastman Kodak for the latest revision.

Device Name	Available Part Numbers	Features		
KAI-1003M	2H4544	Monochrome	Microlens	Sealed
KAI-1003M	2H4825	Monochrome	Microlens	Taped Cover Glass
KAI-1003	2H4828	Monochrome	-	Taped Cover Glass